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HARDWARE IMPLEMENTATION OF AN ANALOG SPIKING NEURON WITH DIGITAL CONTROL OF INPUT SIGNALS WEIGHING

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ABSTRACT

Context. Significant challenges facing hardware developers of artificial intelligence systems force them to look for new non-standard architectural solutions. One of the promising solutions is the transition from von Neumann's classic architecture to neuromorphic architecture, which at the hardware level tries to imitate the work of the neural network of the human brain. A neuromorphic processor built as hardware implementation of a spiking neural network consists of a large number of elementary electronic circuits that structurally and functionally correspond to neurons. Thus, the design of hardware implementation of a spiking neuron as the basic building element of a neuromorphic processor is of great scientific interest.

Objective. The goal of the work is to design an analog spiking neuron hardware implementation with digital control of input signals by binary synaptic weighting coefficients.

Method. Designing is performed at the logical/schematic and topological levels of the design flow using modern tools of electronic design automation. All proposed schematic and layout solutions are verified and simulated using computer aided design tools to prove their functionality.

Results. The schematic and layout solutions have been developed and investigated for the hardware implementation of the spiking analog neuron with digital control of input signals by binary synaptic weighting coefficients to be the basic building element of a spiking neural network of the neuromorphic processor.

Conclusions. The proposed hybrid design of the spiking neuron hardware implementation benefits by combining the simplicity of analog signal processing methods in the neuron with digital control of the state of the neuron using binary weighting coefficients. The simulation results confirm the functionality of the obtained schematic/layout solutions and demonstrate the possibility of implementing logical functions inherent in the perceptron. The prospects for further research may include the design of hardware implementation for a spiking neural network core based on the developed schematic and layout solutions for the spiking neuron.

KEYWORDS: neuromorphic processor, spiking neural network, neuron, synaptic coefficient, layout design.

ABBREVIATIONS

AI is artificial intelligence;
ANN is an artificial neural network;
SNN is a spiking neural network;
VLSI is very large-scale integration;
IC is integrated circuit;
CAD is computer aided design;
EDA is electronic design automation;
DRC is design rule check;
ERC is electrical rule check;
LVS is layout versus schematic;
LIF is leaky integrate-and-fire;
STDP is spike timing dependent plasticity;
GPU is a graphics processing unit;
MOS is metal-oxide-semiconductor;
Si-IPD is silicon-based integrated passive devices;
DC is a direct current.

NOMENCLATURE

V_{DD} is a positive power supply voltage for integrated circuits;

V_{GND} is a zero voltage reference point in the circuit used as a baseline for measuring the voltage of other circuit components;

$V_{\text{base.}}$ is a reference voltage for the excitatory or inhibitory circuits of the synaptic input;

V_{offset} is a decremental or incremental voltage for the excitatory or inhibitory circuits of the synaptic input;

w_i is a synaptic weighting coefficient of the i-th synaptic input of the neuron.

INTRODUCTION

The growing interest in building AI systems based on neural networks prompts the search for new architectural solutions for hardware, which would be more adequate to the methods of solving problems in the neural network basis. It becomes clear that using arrays of graphics processors for the hardware of AI systems has significant limitations in terms of energy efficiency, autonomy, mobility, scalability, etc., and can only be considered as a temporary solution. Therefore, in recent years, more and more attention has been drawn to neuromorphic computer systems that are built and function similarly to the biological neural network of the human brain. A neuromorphic processor in such a system is a VLSI circuit organized as a spiking neural network of computing elements that functionally correspond to neurons. The design of neuromorphic processors, their basic elements and the hardware implementation of neuromorphic calculations is an actual problem of modern computer engineering.

The object of study is the process of signal processing control in the hardware implementation of the analog spiking neuron.

The subject of study is the methods for the design and verification of the hardware implementation of the analog spiking neuron for a neuromorphic processor neural network.

The purpose of the work is to develop and study schematic and layout solutions for the hardware implementation of the analog spiking neuron with the digital

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control of input signals by binary synaptic weighting coefficients.

1 PROBLEM STATEMENT

The key problem of neuromorphic computing is the design and fabrication of neuromorphic chips based on the hardware implementation of spiking neurons and spiking neural networks as VLSI circuits [1, 2]. The spiking neural network of a neuromorphic processor can be built based on the use of analog or digital circuits [3–6]. Both approaches have some advantages and drawbacks. But the best option would rather be a hybrid circuit as a combination of analog and digital parts. The optimal choice for the hardware implementation of a neuromorphic processor is the LIF model of the spiking neuron. In [7, 8], a simple implementation of the synapse of the LIF model of an analog spiking neuron was proposed, which uses circuits of parallel-connected MOS transistors that control the current at the output of the synapse to weigh the input signals. However, no method has been proposed to control the weighing of input signals based on the values of the weighting coefficients. That is why the problem is to design the hardware implementation of a spiking analog neuron with digital control of input signals weighing based on the synaptic input model described in [7]. The hardware implementation of the hybrid spiking neuron must be designed at the schematic and layout level of the VLSI design flow using CAD tool Tanner EDA with appropriate verification procedures.

2 REVIEW OF THE LITERATURE

Growing demands of modern AI systems reveal problems and limitation their hardware implementation based on traditional architecture solutions. Using supercomputers and GPU arrays as the hardware platform of AI systems results in the problems of huge energy consumption, limited scalability, and the lack of autonomy. In recent years, it has become obvious that the most promising way to solve these problems would be the transition to neuromorphic systems. Such systems at the hardware level implement the concept of spiking neural networks for the organization of massive parallel processing of information.

Spiking neural networks belong to the third generation of neural networks. SNN is a type of artificial neural network that mainly relies on methods of transmitting and processing information in the form in which they exist in the biological nervous system. As in its biological original, in a SNN, information is transmitted through connections between neurons using short pulses – spikes, which are generated by neurons when they are activated. In the biological nervous system, a spike corresponds to a nerve impulse.

An important feature of the SNN is the asynchronous nature of the work of neurons, due to which there is no constant flow of data across all synaptic connections between neurons, as in a conventional artificial neural network. Each neuron in SNN works independently of the others, responding only to the arrival of a spike from one of the pre-synaptic neurons by changing the membrane potential. This event-driven and asynchronous nature of the work makes it possible to build an energy-efficient hardware implementation of a spiking neural network as a neuromorphic chip.

The method of processing spikes in an artificial neuron depends on the neuron model used in the spiking neural network. There are various models [9] of the neuron, many of which have been implemented in hardware, which can be divided into biologically plausible, biologically inspired, integrate-and-fire models, and derivatives of the original McCulloch-Pitts model. Biologically plausible models such as Hodgkin-Huxley model [10] try to describe the physical processes in the biological neuron as accurately as possible in terms of ion's transferring mechanism through the neuron cell membrane. Biologically inspired models are simplified variants of the Hodgkin-Huxley model, for example, Fitzhugh-Nagumo [11], Hindmarsh-Rose [12] models, or the popular Izhikevich spiking neuron model [13], which accurately model the behavior of the biological neuron rather than its physical activity. Although those models are more computation-oriented and have a simpler hardware implementation than for the Hodgkin-Huxley model, they are still too complex to practically build neuromorphic systems based on them.

Less biologically realistic and more computationally simple are a set of integrate-and-fire models of the spiking neuron. These models and their more advanced variant – Leaky Integrate-and-Fire model offer a balance between the accuracy of the description of the neuron's behavior and the simplicity of calculations [14].

The dynamics of the LIF model of a neuron is illustrated in Fig. 1 [15]. Spikes from pre-synaptic neurons are first modulated by the weights of synaptic inputs, then currents at synaptic inputs are integrated into the membrane potential of the neuron, which exponentially decreases over time due to leakage. If the membrane potential exceeds the threshold value, the neuron generates an action potential in the form of a post-spike, after which the membrane potential decreases to the level of the resting potential.

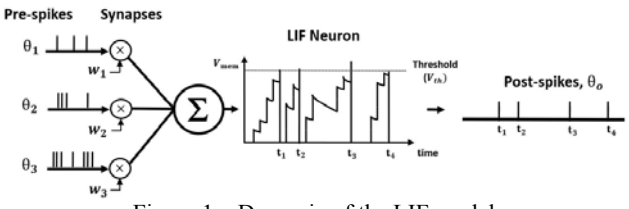

Figure 1 – Dynamic of the LIF model

The behavior of LIF model accurately imitates biological neural network dynamic. That is why this model of a spiking neuron is currently the most popular in the hardware implementation of neuromorphic systems.

Classical ANN training methods based on the back-propagation algorithm, are hardly applicable to spiking

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neural networks, since the SNN is digital in nature, and in addition, backpropagation does not comply with the principle of biological plausibility. That is why there are two approaches to train SNN. First one is the method of Spike Timing Dependent Plasticity [16] based on the principle of locality [17]. According to this method the synapses which activate the post-synaptic neuron shortly after receiving spikes increase their weight, while the synapses that received spikes shortly after post-synaptic neuron activation decrease their weights. The STDP method is ready for the hardware implementation of learning mechanisms and makes it possible to train SNN directly on the neuromorphic chip. The second approach [18,19] applies the method of out-of-chip training that implies the construction of the classical ANN as a continuous analogue of the SNN and teaching this auxiliary network using backpropagation method with a host computer. After training, obtained synaptic weight coefficients are translated into synaptic memory on the neuromorphic chip.

For more than two decades of research in the field of neuromorphic systems and computing, there have been several significant projects, most of which continue to this day [17]. One of the first projects was SpiNNaker, launched in 2011 at the University of Manchester and continued as a part of the European Human Brain Project on the SpiNNaker 2 hardware platform [20]. The SpiNNaker is not a neuromorphic processor but it is rather a massively parallel computing system that was specially built for simulating a spiking neural networks to model human brain structures. The first industrially produced neuromorphic chip was the TrueNorth chip [21], created in 2014 by IBM under the auspices of the DARPA SyNAPSE program. The spiking neurons of the chip cores were built as simplified digital circuits that allow only addition and subtraction operations to be performed. Synaptic weight coefficients were coded with 2-bit values, that is why only out-of-chip training was possible using a different hardware platform with the translation of weight coefficient values obtained as training results into synaptic memory of the TrueNorth chip. The first neuromorphic chip with the ability to learn directly on the chip was the Liohi chip [22] created by Intel in 2018 using a 14 nm technological process, and the Liohi 2 chip that was presented in 2021 and was already made by a 7 nm technology. Synaptic weights in the Liohi chip can already be encoded with 8-bit values, which makes it possible to perform on-chip training. Synaptic weights are modified in the process of local training according to the rule of synaptic plasticity, which is formulated in the form of a simple formula with only addition and multiplication operations implemented in a set of microprograms. The Tianjic neuromorphic chip presented by Beijing Xinhua University in 2019 became the first hybrid chip that combines the architecture of the classical artificial neural network and the spiking neural network in one neuromorphic system. [23,24]. The Tianjic chip is not designed for on-chip training. Therefore, training is carried out on the platform of graphic processors, and the results of training are implemented in the synaptic memory of the chip.

There are other successful projects in the field of development of neuromorphic systems and their number is constantly increasing. The commercial success of artificial intelligence systems that we have observed in recent years and the apparent inability to support this success with adequate hardware platforms leads to the need for further research in the field of neuromorphic systems and their hardware implementation.

3 MATERIALS AND METHODS

Let's consider the block diagram of an analog spiking neuron shown in Fig. 2. The neuron circuit contains a Schmidt trigger that implements the threshold function of activation and a ring oscillator that generates spikes. A leaky integrator forms the membrane potential of the neuron, ensuring the accumulation of the potential to a threshold value upon the arrival of input signals and its gradual reduction to the resting potential in the absence of input spikes. The addition of input signals in the analog neuron is carried out as the usual sum of currents in an electric circuit.

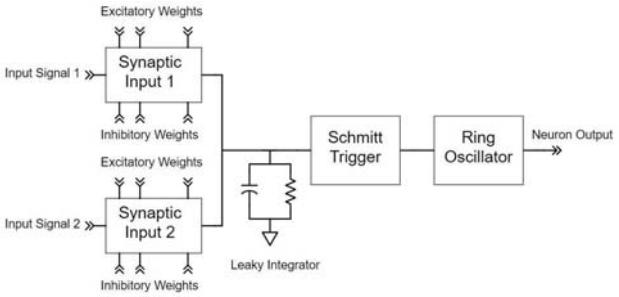

Figure 2 – Block diagram of an analog spiking neuron with two synaptic inputs [25]

But the most significant components of the neuron are the synaptic inputs, which produce weighted input signals that are amplified or attenuated according to the values of the synaptic weights. To weigh the input signal, the hardware implementation of the synapse has been proposed in [7,8] which uses excitation and inhibition circuits consisting of several MOS transistors connected in parallel, as shown in Fig. 3.

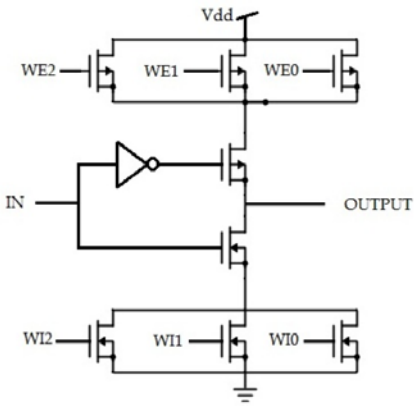

Figure 3 – Circuit diagram for the synaptic input [7]

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By changing the voltage levels on the gates of the transistors in the excitation and/or inhibition circuits, the input signal can be weighted. This can be done by alternately switching these transistors to the subthreshold mode of operation, which allows us to gradually increase or decrease the current at the synapse output. Regardless of the number of transistors in the circuits, it is sufficient to use two voltage levels – V_{base} and V_{offset}, where $V_{DD} \geq V_{base} > V_{offset}$ for the excitation circuit, and $V_{GND} \leq V_{base} < V_{offset}$ for the inhibition circuit, which are alternately applied to the gates and switch the transistors one by one in the subthreshold mode of operation. Three MOS transistors in the excitation and inhibition circuits, as shown in Fig. 3, provide a possibility to obtain four levels of current at the synapse output and, accordingly, four levels of the post-synaptic potential at the leaky integrator.

The selection of the post-synaptic potential level is carried out by switching the gates of the transistors in the excitation and/or inhibition circuits with one of two power sources – V_{base} or V_{offset}. To control this selection for excitation and inhibition circuits consisted of three MOS transistors, 2-bit values can be used acting as synaptic weighting coefficients.

The circuit diagram for digital control of voltage on the gates of MOS transistors in the excitation and inhibition circuits is shown in Fig. 4, with voltage switches built on two transmission gates [26].

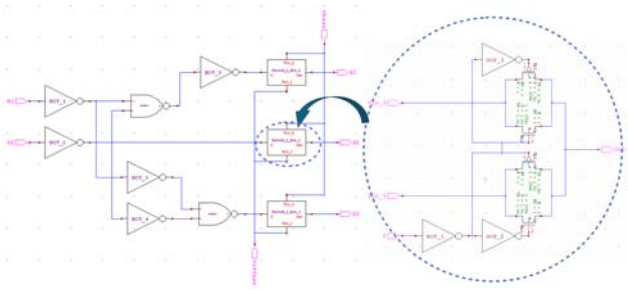

Figure 4 – Circuit diagram for the digital control of voltage

The layout design of the voltage control circuit is demonstrated in Fig. 5.

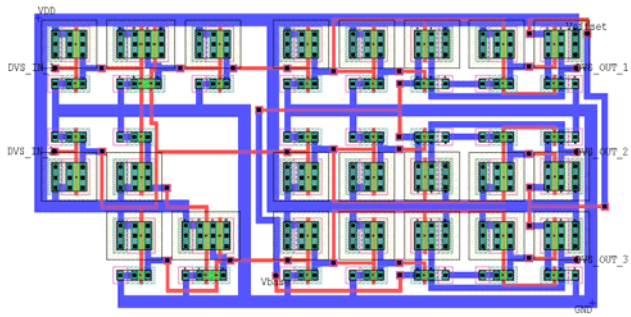

Figure 5 – Layout design of the voltage control circuit

The circuit diagram of the synaptic input with two blocks of digital control with excitatory and inhibitory weighting coefficients is shown in Fig. 6. Unlike a biological neuron, this hardware implementation allows us to use both excitatory and inhibitory weighting coefficients, which adds additional functional flexibility to such a neuron implementation.

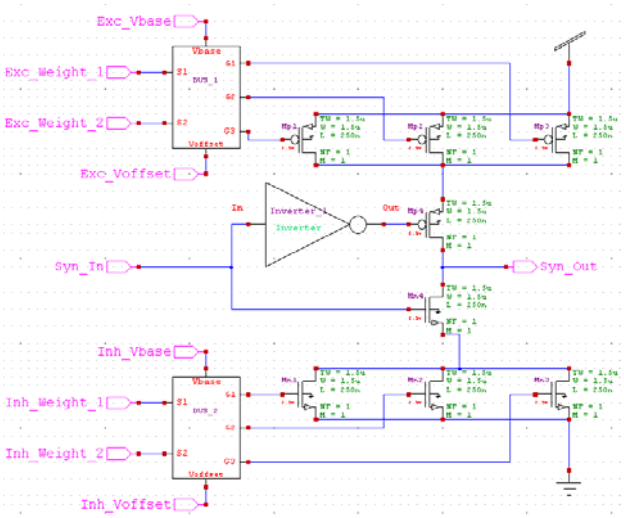

Figure 6 – Circuit diagram for the synaptic input with the digital control of input signal by synaptic weights

The advantage of the analog implementation of the neuron is the simplicity of adding new synaptic inputs to the neuron, since the summation of weighted input signals occurs naturally according to Kirchhoff's law as the sum of currents.

For the hardware implementation of the threshold activation function, a Schmitt trigger is used, based on the circuit on MOS transistors, as shown in Fig. 7. The Schmitt trigger converts the analog input signal of the membrane potential into a digital output signal that activates a spike generator if the membrane potential of the neuron exceeds the threshold level. A classic ring oscillator consisting of an odd number of inverters arranged in a ring is used as a spike generator.

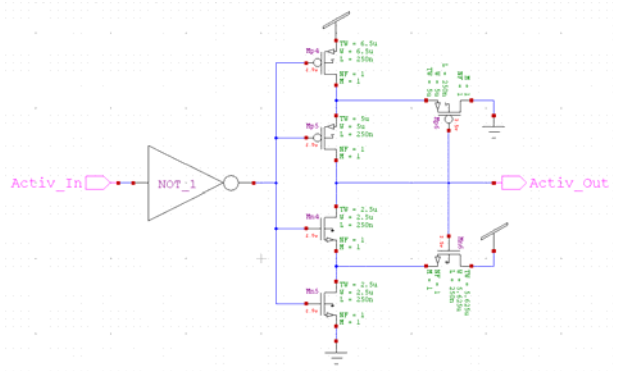

Figure 7 – Circuit diagram of the Schmitt trigger

The layout design of the neuron activator based on the Schmitt trigger and the generator of spikes based on the ring oscillator are shown in Fig. 8 and Fig. 9, respectively.

Based on the developed components of the spiking neuron, a neuron circuit with two synaptic inputs was designed in accordance with the block diagram shown in

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Fig. 2. The layout design of the neuron with two synaptic inputs and the digital control of input signals weighing by binary synaptic weighting coefficients is shown in Fig. 10. It should be noted that capacitive and resistive elements of the leaky integrator are formed on the back side of the silicon wafer using 3D Silicon-based Integrated Passive Devices (Si-IPD) technology and through-silicon vias used to integrate passive components such as inductors, resistors and capacitors on a chip. The characteristics of those elements were directly added to the netlist exported from the neuron layout for its verification.

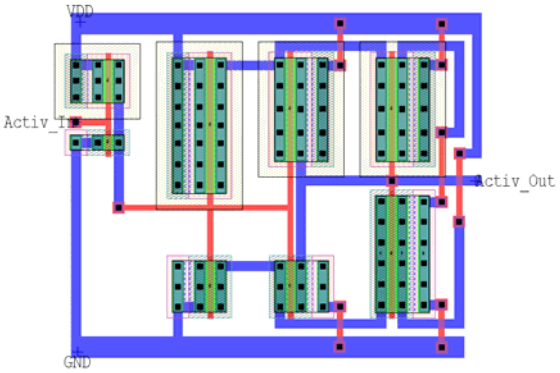

Figure 8 – Layout design of the Schmitt trigger

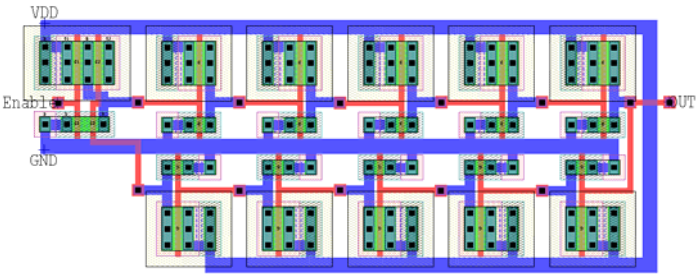

Figure 9 – Layout design of the ring oscillator

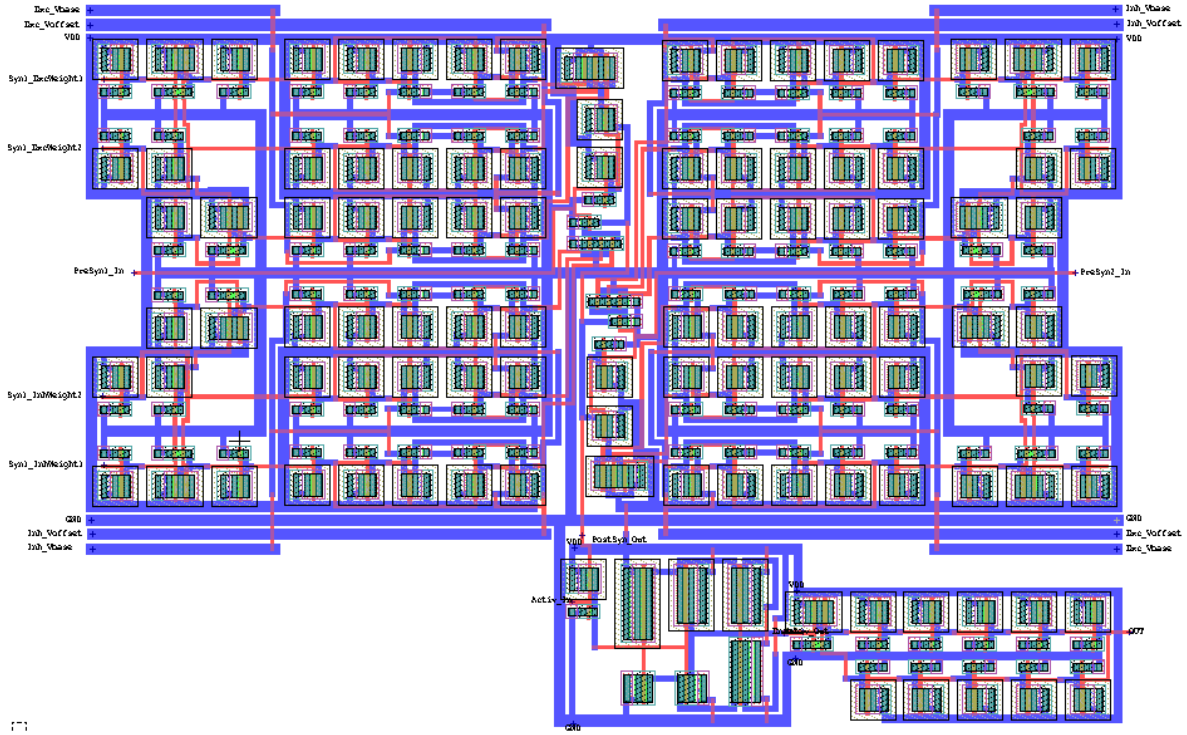

Figure 10 – Layout design of the analog spiking neuron with two synaptic inputs and digital control of input signals weighing

4 EXPERIMENTS

The spiking analog neuron hardware implementation is designed using Tanner EDA software which is a professional standard in the field of VLSI design. The Tanner EDA provides a complex software solution for the design and verification at the schematic and layout levels of the design flow for full-custom analog and mixed signal integrated circuits. The design flow can be demonstrated using the diagram shown in Fig. 11.

After defining circuit specifications, a logic/transistor circuit is designed at schematic level using S-Edit component of Tanner EDA. To simplify the design of larger structures, a symbolic designation (Symbol) is created and associated with the circuit. Simulation of the circuit at the schematic level is carried out to determine its functionality and, in case of errors, the circuit is revised. The verified circuit is exported to the netlist of schematic level.

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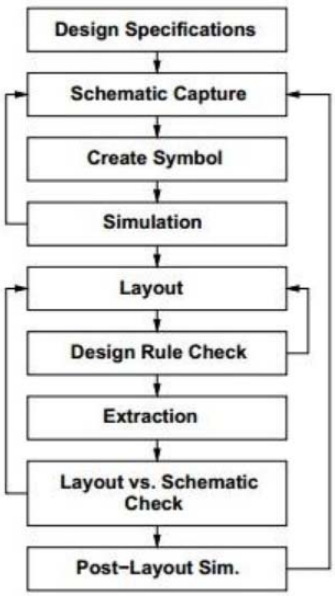

Figure 11 – Design flow diagram

According to the transistor circuit, a topological drawing (Layout) of the placement of diffusion areas of transistors, gates, interconnects, power buses, etc. on a silicon crystal is developed using L-Edit component of Tanner EDA. Layout verification is carried out for compliance with design rules and technological standards using Design Rule Check, (DRC) and Electrical Rule Check (ERC) procedures. If non-compliance with the design rules is detected, the layout design is corrected.

Next, the layout is exported to the netlist of the layout level and is verified by comparing the netlists of the schematic and layout levels using Layout versus Schematic Check (LVS) component. When inconsistencies are detected, the layout design is redone. At the final stage of design flow, Post Layout Simulation is carried out at the layout level to compare with that of schematic level. Simulation results at schematic and layout levels are obtained as waveform probing of signals at reference nodes of the circuit.

5 RESULTS

It is well known that a neuron with two inputs is an elementary perceptron capable of implementing simple logical functions. Let's investigate the functionality of proposed schematic solutions using the example of calculating logical functions.

We will apply periodic signals to the pre-synaptic inputs of the neuron, which provide all four binary combinations possible for a device with two inputs. Waveforms probing is registered at some reference nodes of the neuron as input signals, membrane potential of the neuron, activation signal and output signal of the neuron. Since synaptic weighting coefficients are two-bit binary values, it is easy to estimate the effect of all possible combinations of weighting coefficients of the synaptic inputs on the output signal of the neuron. Assume that the input signals are affected only by the excitatory weighting coefficients of the synaptic inputs. Then, for a neuron with two synaptic inputs, we have sixteen possible combinations of two-bit weighting coefficients w_1 and w_2.

Some simulation results for combinations of excitatory synaptic weighting coefficients which provide the implementation of different logical functions are shown in Fig. 12 as signal waveforms at reference nodes of the neuron.

The generalized result of modeling the neuron's processing of input signals for sixteen combinations of excitatory synaptic weighting coefficients with interpretation in terms of logical functions is shown in Table 1 where A and B stand for signals at the pre-synaptic inputs.

Table 1 – Logical functions generated at neuron's output

w_2	w_1	Neuron Output
00	00	0
00	01	A AND B
00	10	A
00	11	A
01	00	A AND B
01	01	A AND B
01	10	A
01	11	A
10	00	B
10	01	B
10	10	A OR B
10	11	A OR B
11	00	B
11	01	B
11	10	A OR B
11	11	A OR B

To implement the logical NOT function, it is necessary to use inhibitory weighting coefficients. The input signal to be inverted is applied to the first synaptic input of the neuron, while at the same time the second input is applied with DC signal whose level corresponds to V_{DD} value. The signal at the first synaptic input is affected by inhibitory weighting coefficient only while the signal at the second synaptic input is neither amplified nor inhibited. The signal waveforms at the reference nodes of the neuron are shown in Fig. 13 for inhibitory weighting coefficient of the first synaptic input w_1=10 while the others weighting coefficients are zero.

Thus, the designed circuit of an analog neuron with digital control of input signals weighing using binary synaptic coefficients acts as an elementary perceptron and can implement logical functions AND, OR and NOT.

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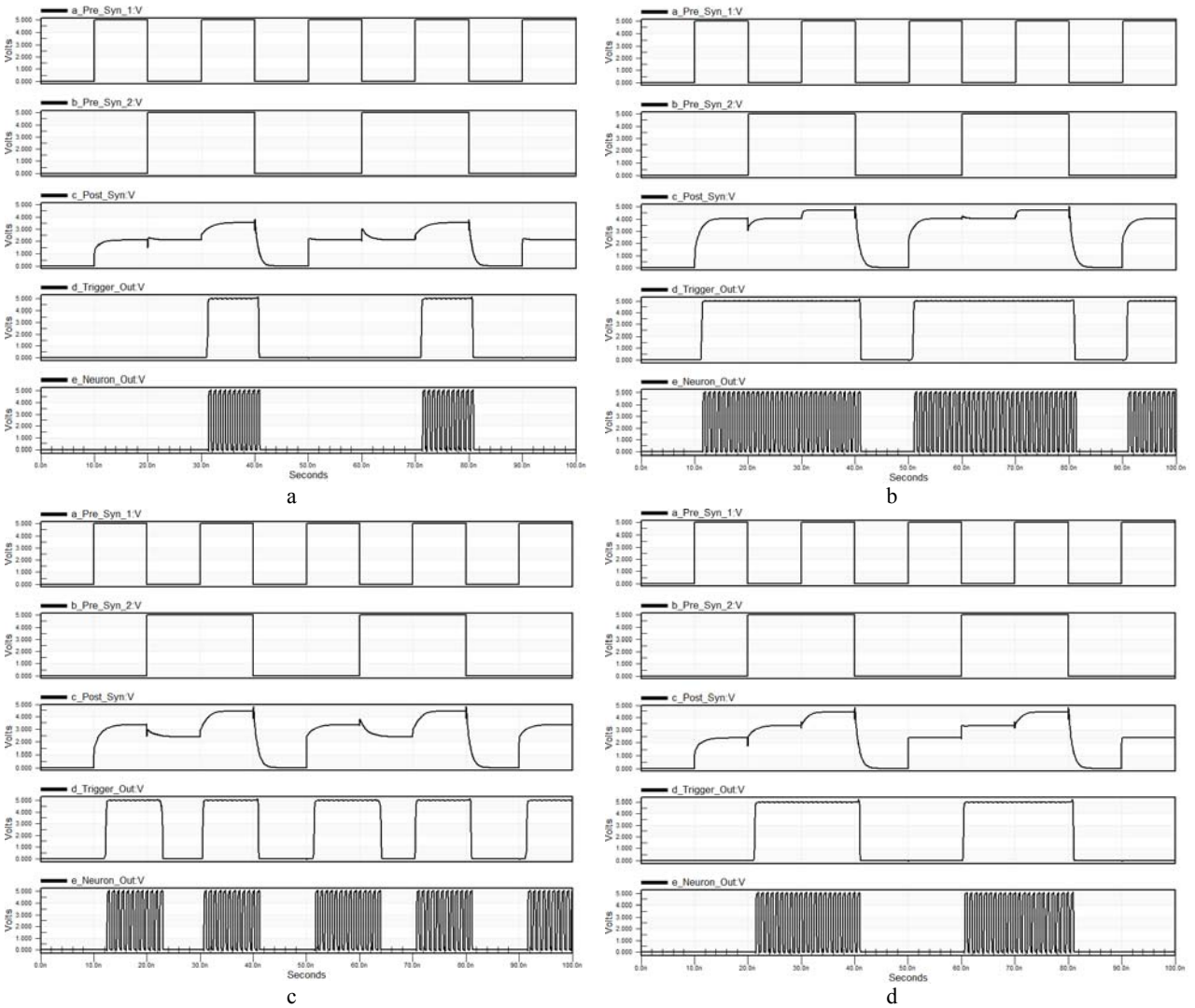

Figure 12 – Signal waveforms at reference nodes of the neuron for some combinations of weighting coefficients: a – w_1=01, w_2=01, Out = A AND B; b – w_1=11, w_2=11, Out = A OR B; c – w_1=10, w_2=01, Out = A; d – w_1=01, w_2=10, Out = B

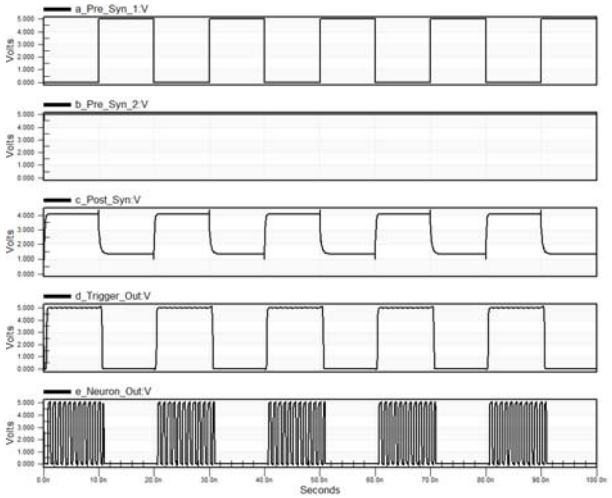

Figure 13 – Logical NOT function implementation using inhibitory weighting coefficient w_1=10

6 DISCUSSION

The spiking neuron is a node of a spiking neural network that forms a neuromorphic chip. That is why the spiking neuron can be considered as a basic building element for the neuromorphic processor. The main results of the paper are schematic and layout solutions for the hardware implementation of an analog spiking neuron with digital control of input signals weighing. Analog nature of the neuron allows us to simplify signal processing implementation, but the state of the neural network should be saved as digital values of weighting coefficients in distributed memory devices. This fact determines requirements to provide the digital control of input signals weighing using binary values of weighting coefficients.

The proposed solutions are based on the synaptic input schematic described in [7] which is the closest analogue to the considered hardware implementation. In [7], authors discus simple approach to weigh input signals using the excitation and inhibition circuits consisted of parallel connected *p*-type and *n*-type MOS transistors. But any methods to control the amplification and attenuation of

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input signals using synaptic weighting coefficients have not been proposed. In the presented research for the synaptic input the schematic solution is developed to digitally control voltage on the gates of MOS transistors in the excitation and inhibition circuits. This allows us to control input signals of the neuron using binary values of the synaptic weighting coefficients.

The practical significance of the research is related to the layout design of the analog spiking neuron. This design can be used as the basic building block of a semiconductor intellectual property core to produce a neuromorphic chip as an application-specific integrated circuit.

The schematic solutions for all neuron blocks and the neuron as whole are verified by the simulation using CAD tools with obtaining waveforms of signals at reference nodes of circuits. The layout solutions are verified with DRC, ERC, LVS checks and post-layout simulations.

The simulation results obtained for all combinations of two-bit weighting coefficients demonstrate how the neuron processes input signals to calculate logical function which is the classical problem for the perceptron. The weighting coefficients for a specific problem can be found as the result of off-line learning and then translated to two-bit binaries.

The advantage of the proposed hybrid solution for the spiking neuron consists in the simplicity of neuron circuit scaling by adding new synaptic input blocks. The schematics of the neuron core and synaptic input blocks remain the same with adding new inputs to the neuron. That allows us to easily build neuron circuits with multiple inputs for a spiking neuron network of the neuromorphic processor.

The simplicity of scaling the neuron schematic and layout solutions opens up prospects for further research in the direction of developing spiking neural network structures of a neuromorphic processor.

CONCLUSIONS

The problem of controlling the weighing of input signals for an analog spiking neuron using binary synaptic weighting coefficients has been solved.

The scientific novelty of obtained results is that the digital method of controlling the weighing of input signals for an analog spiking neuron is proposed. The hybrid design of the neuron improves the previously developed schematic of the synaptic input making possible to control input signals of the analog neuron using binary values of weighting coefficients. This allows us to use analog nature of signal processing by neurons while the state of neurons is determined by binary values of weighting coefficients stored in memory devices.

The practical significance of obtained results is that the layout is designed for the analog spiking neuron with digital controlling the weighing of input signals by binary synaptic weighting coefficients. This layout design can be used as the SIP core basic building block to produce a spiking neural network of a neuromorphic chip.

Prospects for further research are to develop and study structures of SNN for a neuromorphic processor based on the designed spiking analog neuron with the digitally controlled weighing of input signals.

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АПАРАТНА РЕАЛІЗАЦІЯ АНАЛОГОВОГО ІМПУЛЬСНОГО НЕЙРОНА З ЦИФРОВИМ КЕРУВАННЯМ ЗВАЖУВАННЯМ ВХІДНИХ СИГНАЛІВ

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АНОТАЦІЯ

Актуальність. Значні виклики, що постають перед розробниками апаратного забезпечення систем штучного інтелекту, змушують шукати для реалізації таких систем нові нестандартні архітектурні рішення. Одним із таких перспективних рішень є перехід від класичної архітектури фон Неймана до нейроморфної архітектури, яка на апаратному рівні намагається імітувати роботу нейронної мережі людського мозку. Нейроморфний процесор, побудований як апаратна реалізація імпульсної нейронної мережі, складається з великої кількості елементарних електронних схем, які структурно та функціонально відповідають нейронам. Тому, проєктування апаратної реалізації імпульсного нейрона як основного будівельного елементу нейроморфного процесора представляє собою значний науковий та практичний інтерес.

Мета роботи. Метою роботи є розробка апаратної реалізації аналогового імпульсного нейрона з цифровим керуванням зважуванням вхідних сигналів двійковими синаптичними ваговими коефіцієнтами.

Метод. Проєктування виконується на схемотехнічному та топологічному рівнях наскрізного маршруту проєктування інтегральних схем з використанням сучасних засобів автоматизації проєктування електронних пристроїв. Для підтвердження функціональності усіх запропонованих схемотехнічних та топологічних рішень проведено їх верифікацію та моделювання засобами автоматизованого проєктування,.

Результати. Розроблено та досліджено схемотехнічні та топологічні рішення для апаратної реалізації аналогового імпульсного нейрона з цифровим керуванням зважуванням вхідних сигналів двійковими синаптичними ваговими коефіцієнтами як основного елемента побудови імпульсної нейронної мережі нейроморфного процесора.

Висновки. Запропонована гібридна конструкція апаратної реалізації імпульсного нейрона має переваги завдяки поєднанню простоти аналогових методів обробки сигналів в нейроні з цифровим керуванням станом нейрона за допомогою двійкових вагових коефіцієнтів. Результати моделювання підтверджують функціональність отриманих схемотехнічних та топологічних рішень і демонструють можливість реалізації логічних функцій, притаманних персептрону. Перспективи подальших досліджень можуть включати розробку апаратної реалізації ядра імпульсної нейронної мережі нейроморфного процесора на основі розроблених схемотехнічних та топологічних рішень для імпульсного нейрона..

КЛЮЧОВІ СЛОВА: нейроморфний процесор, імпульсна нейронна мережа, нейрон, синаптичний коефіцієнт, топологічне проєктування.

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